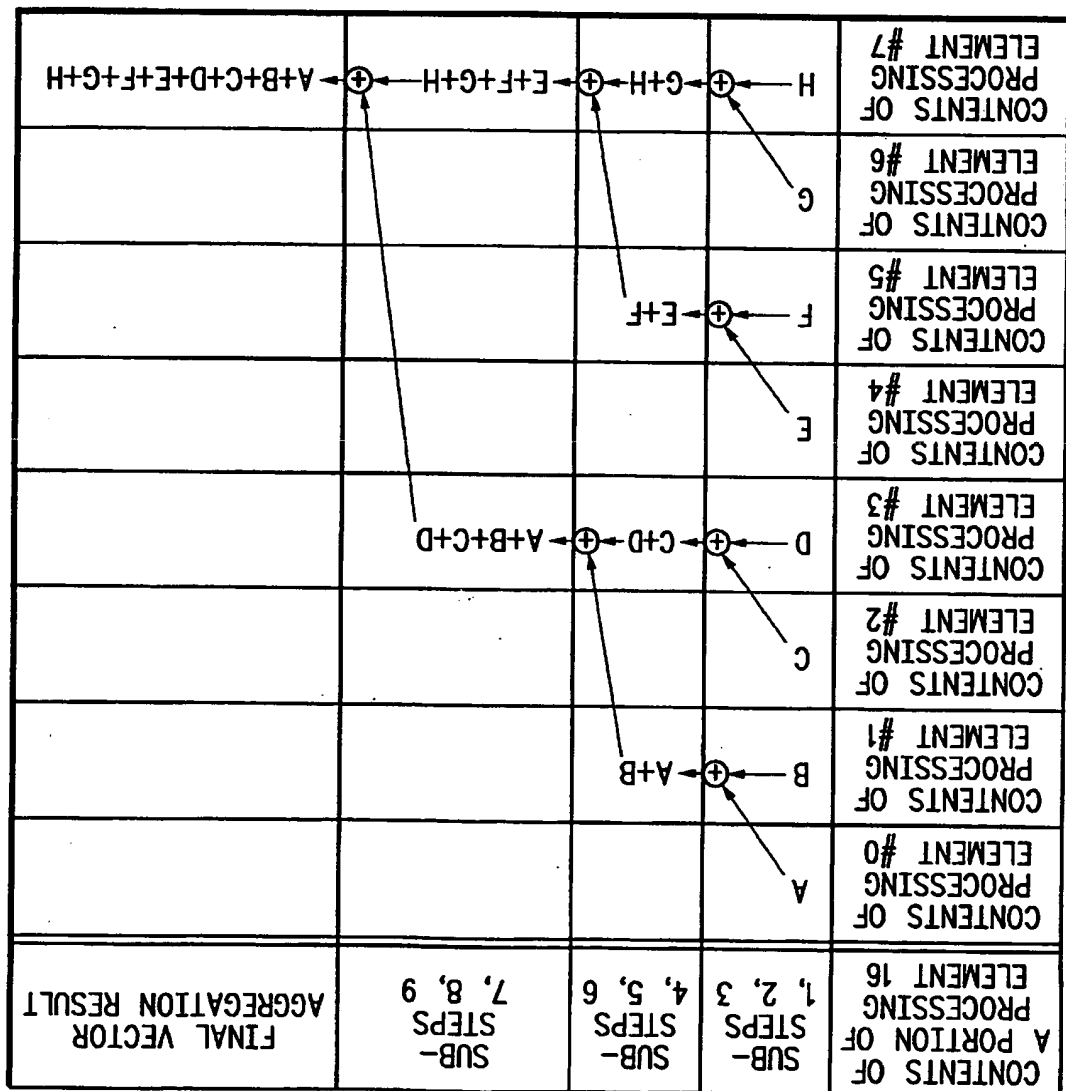


	L #	Hits	Search Text	DBs
1	L1	1130	(fenc\$3 synch\$ barrier) near10 load near10 (instruction operation)	USPAT; US-PGPUB
2	L2	21	1 near50 (load near2 buffer)	USPAT; US-PGPUB
3	L3	2	1 near50 (load near10 global\$2)	USPAT; US-PGPUB
4	L4	344	(fenc\$3 synch\$ barrier) near10 load near10 (instruction operation)	EPO; JPO; DERWENT; IBM_TDB
5	L5	1	4 near50 (load near2 buffer)	EPO; JPO; DERWENT; IBM_TDB
6	L6	1	4 near50 (load near10 global\$2)	EPO; JPO; DERWENT; IBM_TDB
7	L7	4	3 5 6	USPAT; US-PGPUB ; EPO; JPO; DERWENT; IBM_TDB
8	L8	1197	(fenc\$3 sync\$ barrier) near10 load near10 (instruction operation)	USPAT; US-PGPUB
9	L9	21	8 near50 (load near2 buffer)	USPAT; US-PGPUB
10	L12	2	4 and (load near2 buffer)	EPO; JPO; DERWENT; IBM_TDB
11	L14	52	8 and (load near2 buffer) not 2	USPAT; US-PGPUB
12	L16	38	8 and (load near10 global\$2) not (9 14)	USPAT; US-PGPUB
13	L15	46	8 and (load near10 global\$2)	USPAT; US-PGPUB
14	L19	1	4 and (load near10 global\$2)	EPO; JPO; DERWENT; IBM_TDB
15	L18	2	4 and (load near2 buffer)	EPO; JPO; DERWENT; IBM_TDB
16	L21	1	4 and (load\$3 near10 global\$2)	EPO; JPO; DERWENT; IBM_TDB
17	L22	4	8 and (load\$3 near10 global\$2) not 15	USPAT; US-PGPUB



PRIOR ART APPROACH USING SINGLE INSTRUCTION
MULTIPLE DATA (SIMD) PROCESSOR INSTRUCTION STEPS:

1. COPY VECTOR
2. SHIFT COPY 1 PE DOWNWARD
3. ADD SHIFTED COPY TO VECTOR
4. COPY TO VECTOR
5. SHIFT COPY 2 PES DOWNWARD
6. ADD SHIFTED COPY TO VECTOR
7. COPY VECTOR
8. SHIFT COPY 4 PES DOWNWARD
9. ADD SHIFTED COPY TO VECTOR

FIG. 5-12
-PRIOR ART-

	Document ID	U	Title	Current OR
1	US 20030 08425 9 A1	<input type="checkbox"/>	MFENCE and LFENCE micro-architectural implementation method and system	711/163
2	US 20020 19906 7 A1	<input checked="" type="checkbox"/>	System and method for high performance execution of locked memory instructions in a system with distributed memory and a restrictive memory model	711/145
3	US 20020 11214 6 A1	<input checked="" type="checkbox"/>	Method and apparatus for synchronizing load operation	712/219
4	US 20020 08781 0 A1	<input checked="" type="checkbox"/>	System and method for high performance execution of locked memory instructions in a system with distributed memory and a restrictive memory model	711/145
5	US 20010 04218 7 A1	<input checked="" type="checkbox"/>	VARIABLE ISSUE-WIDTH VLIW PROCESSOR	712/2
6	US 66153 38 B1	<input checked="" type="checkbox"/>	Clustered architecture in a VLIW processor	712/24
7	US 66119 00 B2	<input checked="" type="checkbox"/>	System and method for high performance execution of locked memory instructions in a system with distributed memory and a restrictive memory model	711/145
8	US 64635 11 B2	<input checked="" type="checkbox"/>	System and method for high performance execution of locked memory instructions in a system with distributed memory and a restrictive memory model	711/145
9	US 63973 54 B1	<input checked="" type="checkbox"/>	Method and apparatus for providing external access to signals that are internal to an integrated circuit chip package	714/34
10	US 63743 70 B1	<input checked="" type="checkbox"/>	Method and system for flexible control of BIST registers based upon on-chip events	714/39
11	US 62791 00 B1	<input checked="" type="checkbox"/>	Local stall control method and structure in a microprocessor	712/24
12	US 60095 39 A	<input checked="" type="checkbox"/>	Cross-triggering CPUs for enhanced test operations in a multi-CPU computer system	714/30
13	US 60031 07 A	<input checked="" type="checkbox"/>	Circuitry for providing external access to signals that are internal to an integrated circuit chip package	710/316
14	US 59665 15 A	<input checked="" type="checkbox"/>	Parallel emulation system and method	703/21
15	US 59564 77 A	<input checked="" type="checkbox"/>	Method for processing information in a microprocessor to facilitate debug and performance monitoring	714/30
16	US 59564 76 A	<input checked="" type="checkbox"/>	Circuitry and method for detecting signal patterns on a bus using dynamically changing expected patterns	714/30
17	US 58870 03 A	<input checked="" type="checkbox"/>	Apparatus and method for comparing a group of binary fields with an expected pattern to generate match results	714/736
18	US 58812 24 A	<input checked="" type="checkbox"/>	Apparatus and method for tracking events in a microprocessor that can retire more than one instruction during a clock cycle	714/47
19	US 58812 17 A	<input checked="" type="checkbox"/>	Input comparison circuitry and method for a programmable state machine	714/30
20	US 58806 71 A	<input checked="" type="checkbox"/>	Flexible circuitry and method for detecting signal patterns on a bus	340/146 .2
21	US 58676 44 A	<input type="checkbox"/>	System and method for on-chip debug support and performance monitoring in a microprocessor	714/39

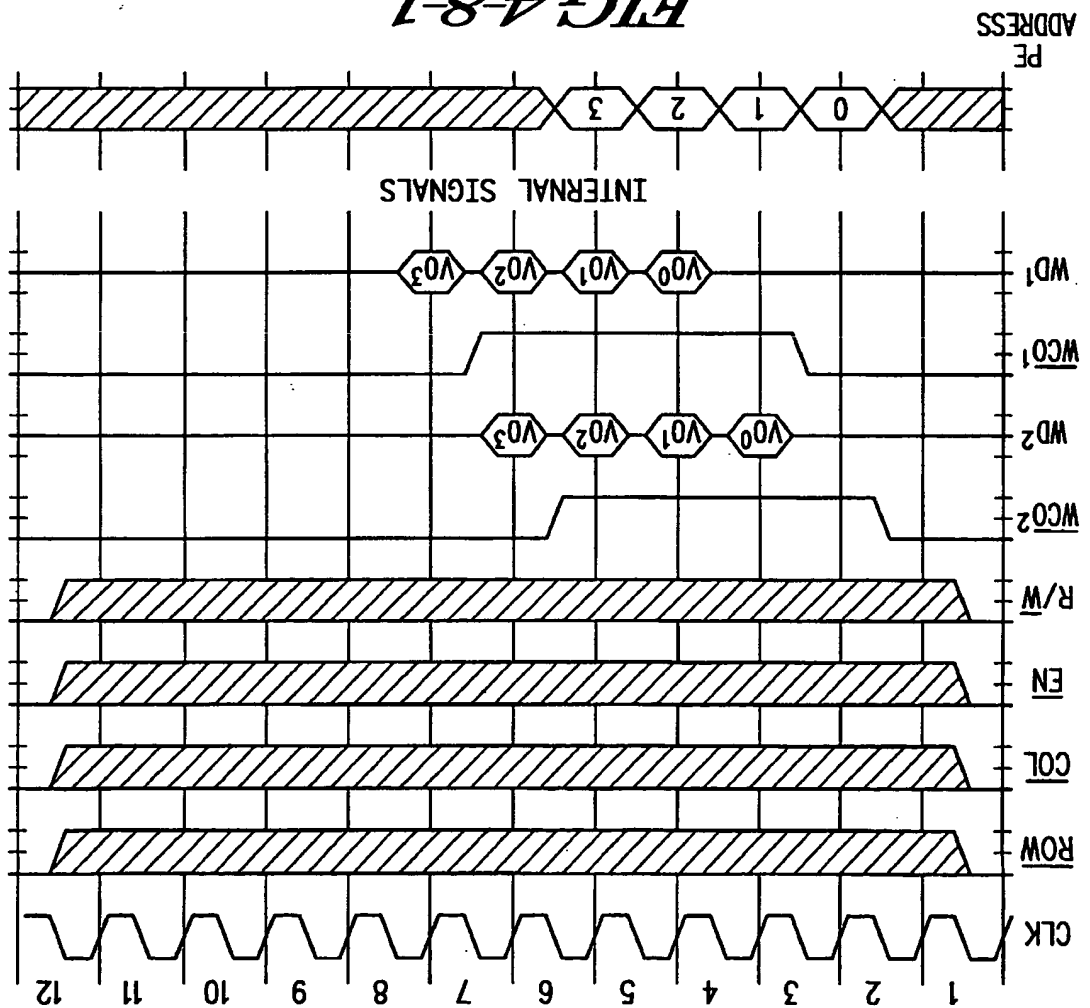


FIG. 4-8-1

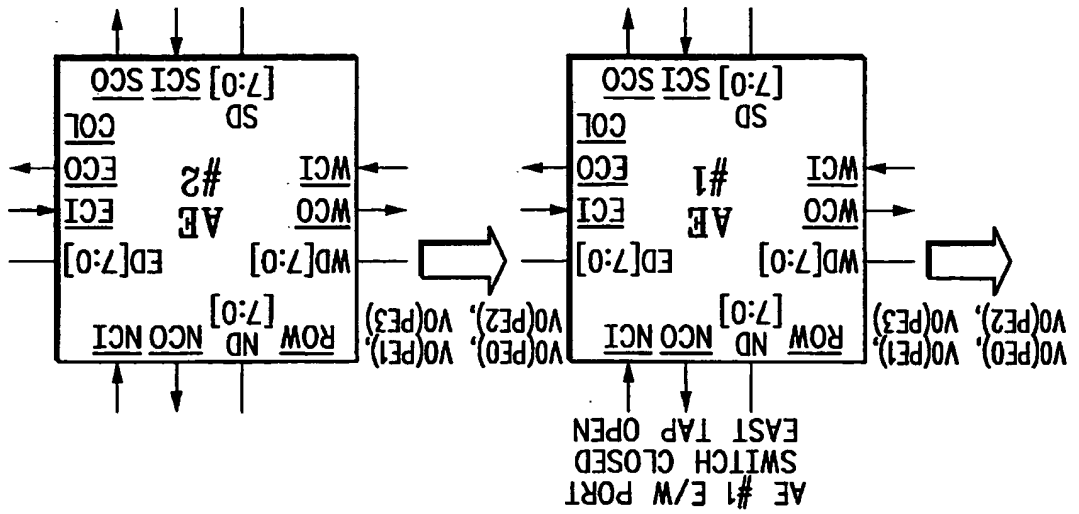


FIG. 4-8-2

□ DON'T CARE

	Docum ent ID	U	Title	Current OR
1	US 20020 11214 6 A1	<input type="checkbox"/>	Method and apparatus for synchronizing load operation	712/219
2	US 60471 22 A	<input type="checkbox"/>	System for method for performing a context switch operation in a massively parallel computer system	709/108
3	US 20030 08425 9 A	<input checked="" type="checkbox"/>	Memory fence and load fence micro-architectural implementation method for speech synthesis, involves dispatching load fencing instruction to cache controller, after removing old loads from memory subsystem	
4	KR 20010 47533 A	<input checked="" type="checkbox"/>	Synchronous memory device	

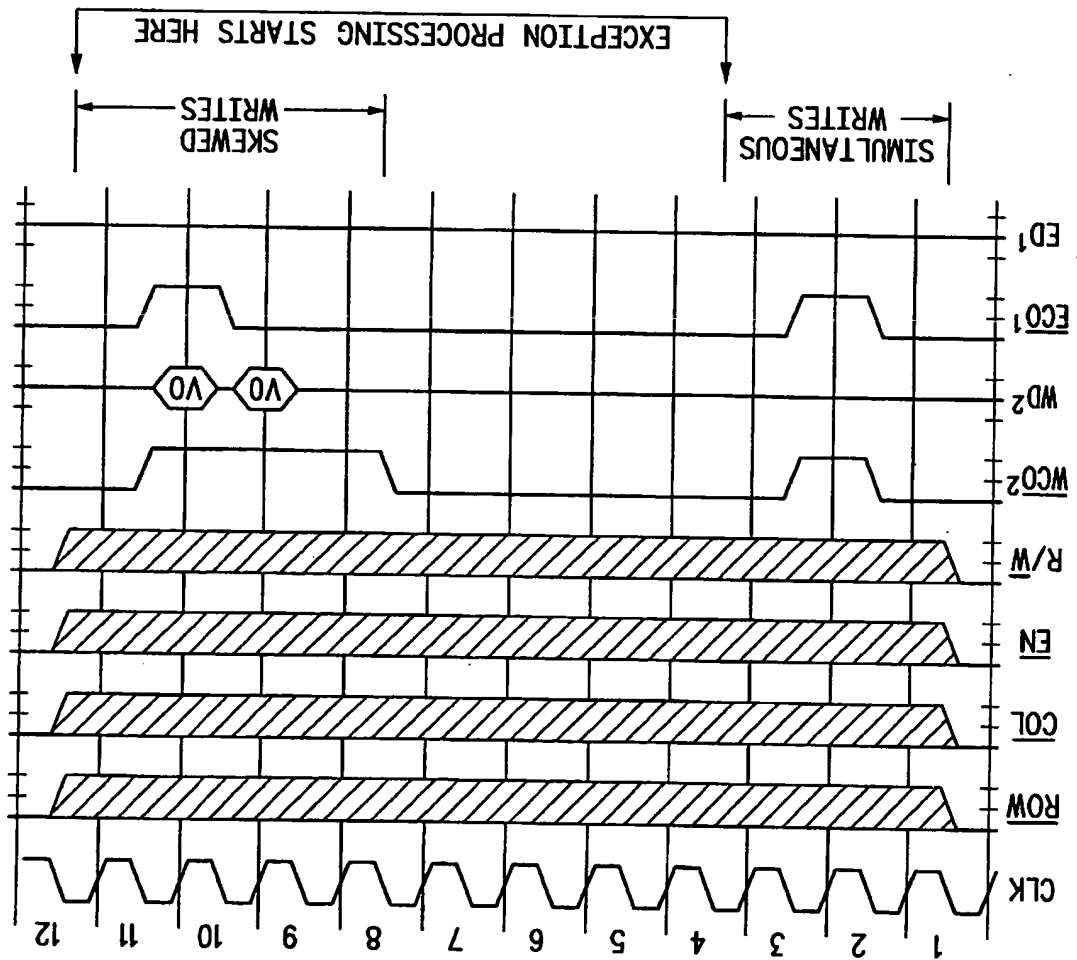


FIG. 4-10-1

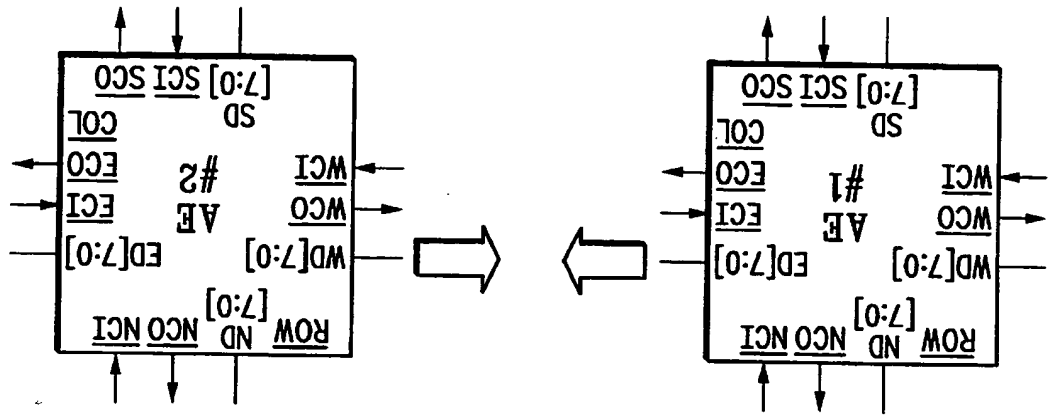


FIG. 4-10-2

DON'T CARE

	Docum ent ID	U	Title	Current OR
1	US 20030 03454 4 A1	<input type="checkbox"/>	Microcomputer	257/523
2	US 20010 03743 4 A1	<input checked="" type="checkbox"/>	Store to load forwarding using a dependency link file	711/146
3	US 66511 51 B2	<input checked="" type="checkbox"/>	MFENCE and LFENCE micro-architectural implementation method and system	711/163
4	US 66292 71 B1	<input checked="" type="checkbox"/>	Technique for synchronizing faults in a processor having a replay system	714/49
5	US 66091 92 B1	<input checked="" type="checkbox"/>	System and method for asynchronously overlapping storage barrier operations with old and new storage operations	712/216
6	US 65499 90 B2	<input checked="" type="checkbox"/>	Store to load forwarding using a dependency link file	711/146
7	US 65464 62 B1	<input checked="" type="checkbox"/>	CLFLUSH micro-architectural implementation method and system	711/135
8	US 64738 37 B1	<input checked="" type="checkbox"/>	Snoop resynchronization mechanism to preserve read ordering	711/146
9	US 64738 32 B1	<input checked="" type="checkbox"/>	Load/store unit having pre-cache and post-cache queues for low latency load memory operations	711/118
10	US 64669 88 B1	<input checked="" type="checkbox"/>	Multiprocessor synchronization and coherency control system	709/248
11	US 64271 93 B1	<input checked="" type="checkbox"/>	Deadlock avoidance using exponential backoff	711/146
12	US 64153 60 B1	<input checked="" type="checkbox"/>	Minimizing self-modifying code checks for uncacheable memory types	711/139
13	US 64143 68 B1	<input checked="" type="checkbox"/>	Microcomputer with high density RAM on single chip	257/523
14	US 63112 61 B1	<input checked="" type="checkbox"/>	Apparatus and method for improving superscalar processors	712/23
15	US 62667 44 B1	<input checked="" type="checkbox"/>	Store to load forwarding using a dependency link file	711/146
16	US 61890 88 B1	<input checked="" type="checkbox"/>	Forwarding stored data fetched for out-of-order load/read operation to over-taken operation read-accessing same memory location	712/216
17	US 61675 09 A	<input checked="" type="checkbox"/>	Branch performance in high speed processor	712/237
18	US 61192 04 A	<input checked="" type="checkbox"/>	Data processing system and method for maintaining translation lookaside buffer TLB coherency without enforcing complete instruction serialization	711/141
19	US 61120 19 A	<input checked="" type="checkbox"/>	Distributed instruction queue	712/214
20	US 60761 58 A	<input checked="" type="checkbox"/>	Branch prediction in high-performance processor	712/230
21	US 60732 10 A	<input checked="" type="checkbox"/>	Synchronization of weakly ordered write combining operations using a fencing mechanism	711/118
22	US 59957 46 A	<input checked="" type="checkbox"/>	Byte-compare operation for high-performance processor	712/220

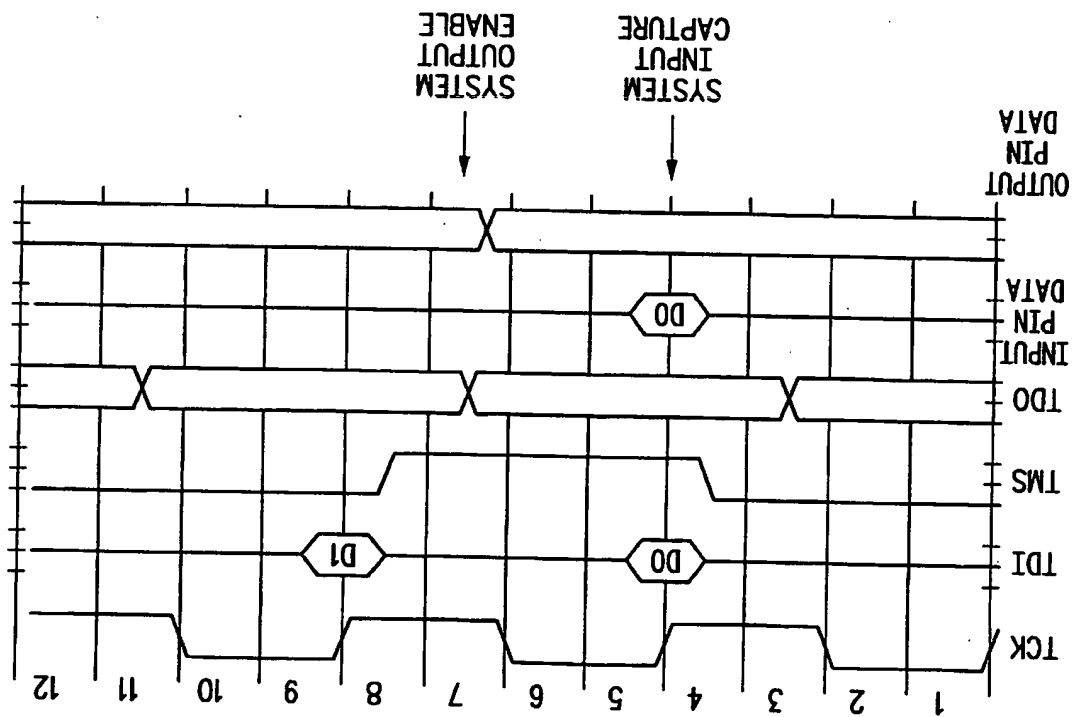


FIG. 4-16

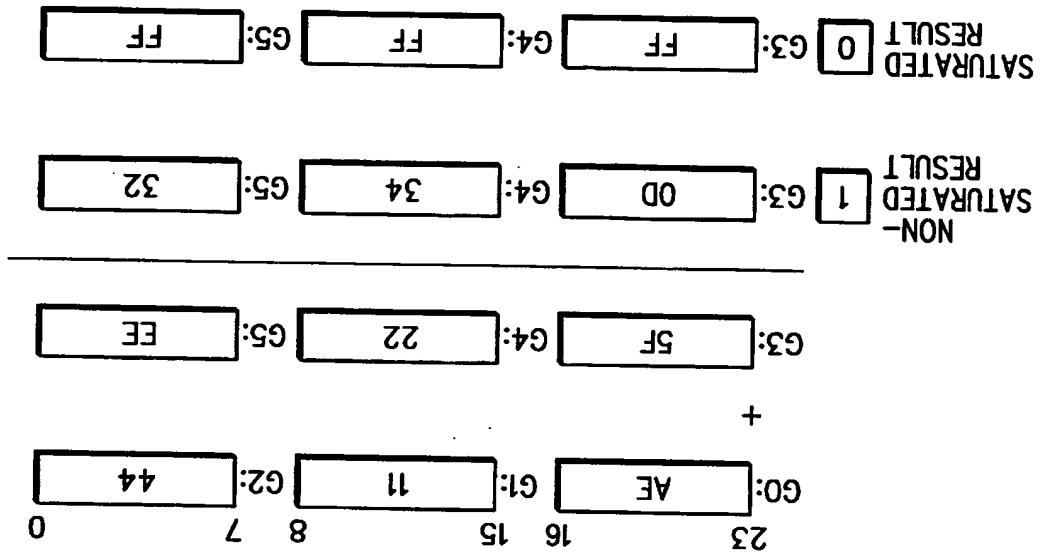
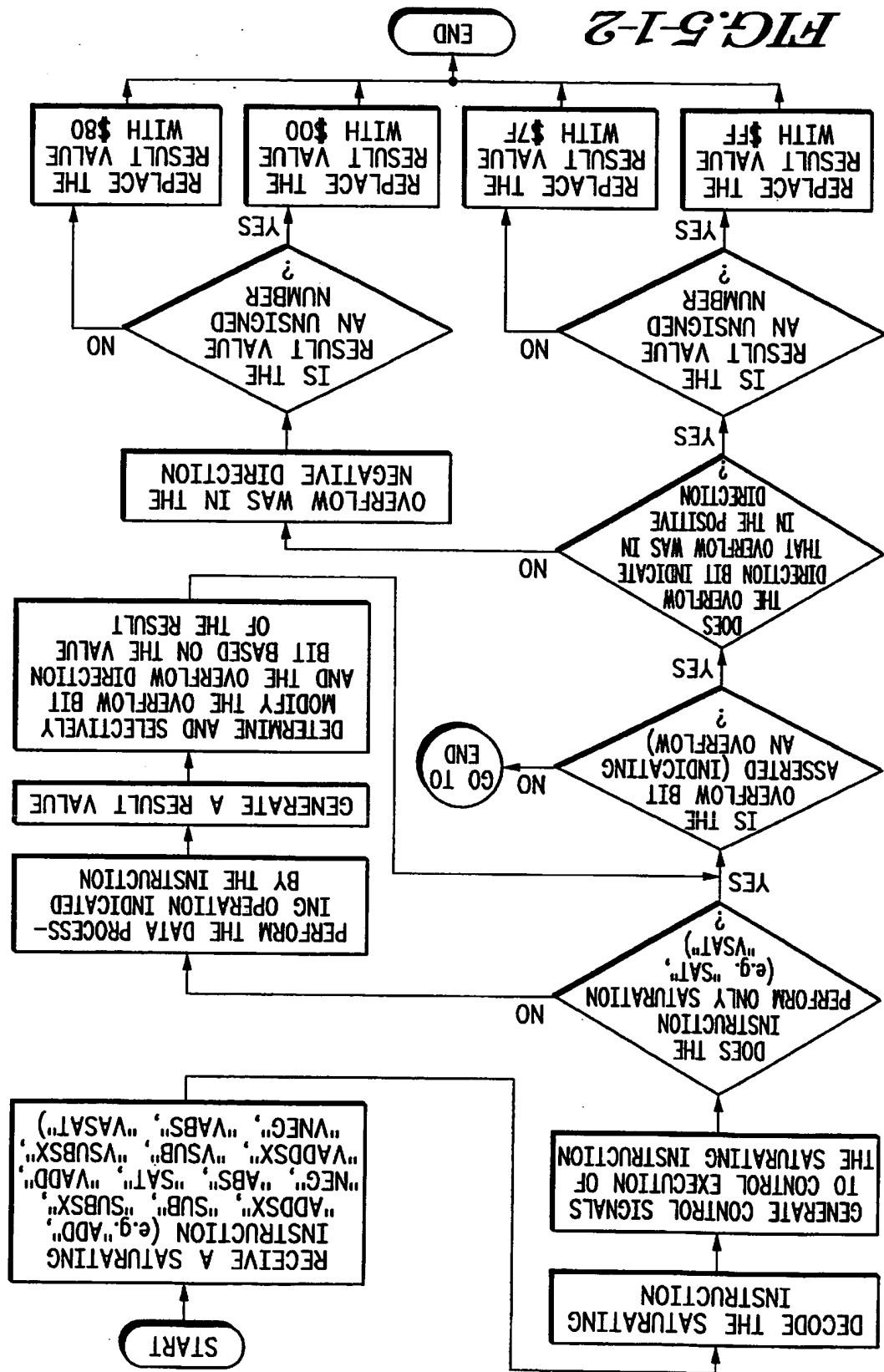


FIG. 5-1-1

	Docum ent ID	U	Title	Current OR
23	US 58812 62 A	<input checked="" type="checkbox"/>	Method and apparatus for blocking execution of and storing load operations during their execution	712/216
24	US 58261 09 A	<input checked="" type="checkbox"/>	Method and apparatus for performing multiple load operations to the same memory location in a computer system	710/39
25	US 57784 23 A	<input checked="" type="checkbox"/>	Prefetch instruction for improving performance in reduced instruction set processor	711/118
26	US 57782 45 A	<input checked="" type="checkbox"/>	Method and apparatus for dynamic allocation of multiple buffers in a processor	712/23
27	US 57245 36 A	<input checked="" type="checkbox"/>	Method and apparatus for blocking execution of and storing load operations during their execution	712/216
28	US 56945 74 A	<input checked="" type="checkbox"/>	Method and apparatus for performing load operations in a computer system	711/140
29	US 55686 24 A	<input checked="" type="checkbox"/>	Byte-compare operation for high-performance processor	712/223
30	US 55064 37 A	<input checked="" type="checkbox"/>	Microcomputer with high density RAM in separate isolation well on single chip	257/373
31	US 54913 59 A	<input checked="" type="checkbox"/>	Microcomputer with high density ram in separate isolation well on single chip	257/373
32	US 54695 51 A	<input checked="" type="checkbox"/>	Method and apparatus for eliminating branches using conditional move instructions	712/239
33	US 54540 91 A	<input checked="" type="checkbox"/>	Virtual to physical address translation scheme with granularity hint for identifying subsequent pages to be accessed	711/203
34	US 54524 67 A	<input checked="" type="checkbox"/>	Microcomputer with high density ram in separate isolation well on single chip	716/1
35	US 54249 69 A	<input checked="" type="checkbox"/>	Product-sum operation unit	708/603
36	US 54106 82 A	<input checked="" type="checkbox"/>	In-register data manipulation for unaligned byte write using data shift in reduced instruction set processor	712/300
37	US 53773 36 A	<input checked="" type="checkbox"/>	Improved method to prefetch load instruction data	712/207
38	US 53677 05 A	<input checked="" type="checkbox"/>	In-register data manipulation using data shift in reduced instruction set processor	712/41
39	US 52436 98 A	<input checked="" type="checkbox"/>	Microcomputer	709/201
40	US 51931 67 A	<input checked="" type="checkbox"/>	Ensuring data integrity by locked-load and conditional-store operations in a multiprocessor system	711/163
41	US 51504 70 A	<input checked="" type="checkbox"/>	Data processing system with instruction queue having tags indicating outstanding data status	712/217
42	US 50310 92 A	<input checked="" type="checkbox"/>	Microcomputer with high density ram in separate isolation well on single chip	711/163
43	US 49759 60 A	<input checked="" type="checkbox"/>	Electronic facial tracking and detection system and method and apparatus for automated speech recognition	704/251
44	US 49673 26 A	<input checked="" type="checkbox"/>	Microcomputer building block	712/21
45	US 48191 51 A	<input checked="" type="checkbox"/>	Microcomputer	709/106



	Docum ent ID	U	Title	Current OR
46	US 47245 17 A	<input checked="" type="checkbox"/>	Microcomputer with prefixing functions	712/210
47	US 47046 78 A	<input checked="" type="checkbox"/>	Function set for a microcomputer	709/106
48	US 46806 98 A	<input checked="" type="checkbox"/>	High density ROM in separate isolation well on single with chip	712/37
49	US 42142 69 A	<input checked="" type="checkbox"/>	Real time digital scan converter	348/442
50	US 39848 14 A	<input checked="" type="checkbox"/>	Retry method and apparatus for use in a magnetic recording and reproducing system	714/16
51	US 37909 58 A	<input checked="" type="checkbox"/>	DATA COMMUNICATION TERMINAL	710/65
52	US 37287 10 A	<input type="checkbox"/>	CHARACTER DISPLAY TERMINAL	345/17

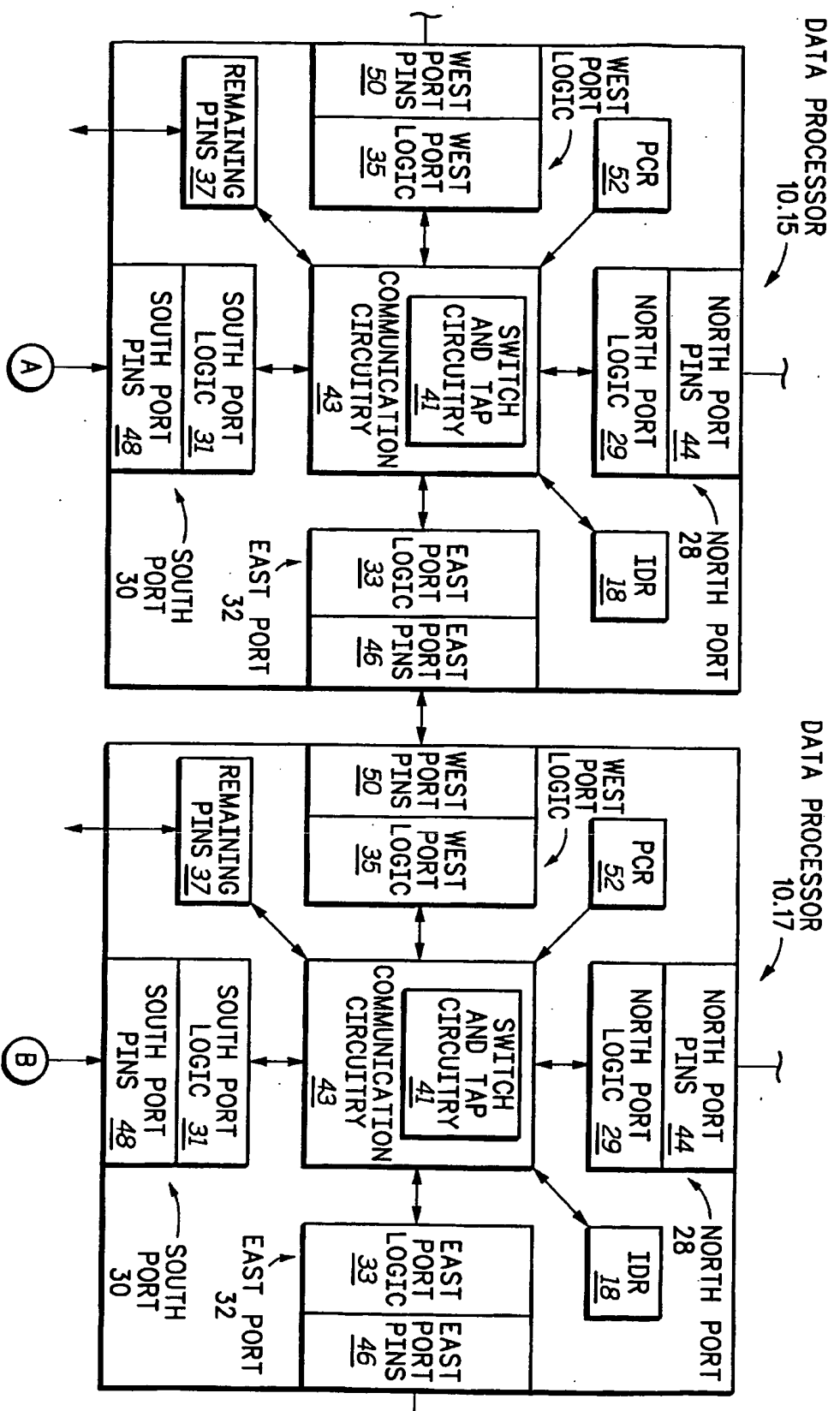


FIG. 5-2-1

	Docum ent ID	U	Title	Current OR
1	US 20030 08425 9 A1	<input type="checkbox"/>	MFENCE and LFENCE micro-architectural implementation method and system	711/163
2	US 20020 19906 7 A1	<input checked="" type="checkbox"/>	System and method for high performance execution of locked memory instructions in a system with distributed memory and a restrictive memory model	711/145
3	US 20020 11214 6 A1	<input type="checkbox"/>	Method and apparatus for synchronizing load operation	712/219
4	US 20020 08781 0 A1	<input checked="" type="checkbox"/>	System and method for high performance execution of locked memory instructions in a system with distributed memory and a restrictive memory model	711/145
5	US 20010 03481 9 A1	<input checked="" type="checkbox"/>	Interleaved data path and output management architecture for an interleaved memory and load pulser circuit for outputting the read data	711/157
6	US 20010 03324 5 A1	<input checked="" type="checkbox"/>	Interleaved memory device for burst type access in synchronous read mode with the two semi-arrays independently readable in random access asynchronous mode	341/200
7	US 66511 51 B2	<input checked="" type="checkbox"/>	MFENCE and LFENCE micro-architectural implementation method and system	711/163
8	US 66119 00 B2	<input checked="" type="checkbox"/>	System and method for high performance execution of locked memory instructions in a system with distributed memory and a restrictive memory model	711/145
9	US 65879 13 B2	<input checked="" type="checkbox"/>	Interleaved memory device for burst type access in synchronous read mode with the two semi-arrays independently readable in random access asynchronous mode	711/5
10	US 64808 18 B1	<input checked="" type="checkbox"/>	Debugging techniques in a multithreaded environment	703/26
11	US 64734 02 B1	<input checked="" type="checkbox"/>	Communications link interconnecting service control points of a load sharing group for traffic management control	370/236
12	US 64704 31 B2	<input checked="" type="checkbox"/>	Interleaved data path and output management architecture for an interleaved memory and load pulser circuit for outputting the read data	711/157
13	US 64635 11 B2	<input checked="" type="checkbox"/>	System and method for high performance execution of locked memory instructions in a system with distributed memory and a restrictive memory model	711/145
14	US 63706 25 B1	<input checked="" type="checkbox"/>	Method and apparatus for lock synchronization in a microprocessor system	711/152
15	US 63538 29 B1	<input checked="" type="checkbox"/>	Method and system for memory allocation in a multiprocessing environment	707/100
16	US 63473 49 B1	<input checked="" type="checkbox"/>	System for determining whether a subsequent transaction may be allowed or must be allowed or must not be allowed to bypass a preceding transaction	710/62
17	US 63144 71 B1	<input checked="" type="checkbox"/>	Techniques for an interrupt free operating system	710/5
18	US 62600 88 B1	<input checked="" type="checkbox"/>	Single integrated circuit embodying a risc processor and a digital signal processor	710/100
19	US 60732 10 A	<input checked="" type="checkbox"/>	Synchronization of weakly ordered write combining operations using a fencing mechanism	711/118
20	US 60700 03 A	<input checked="" type="checkbox"/>	System and method of memory access in apparatus having plural processors and plural memories	710/317
21	US 60471 22 A	<input type="checkbox"/>	System for method for performing a context switch operation in a massively parallel computer system	709/108

STOP MODE SOUTH STREAM ACCESSES

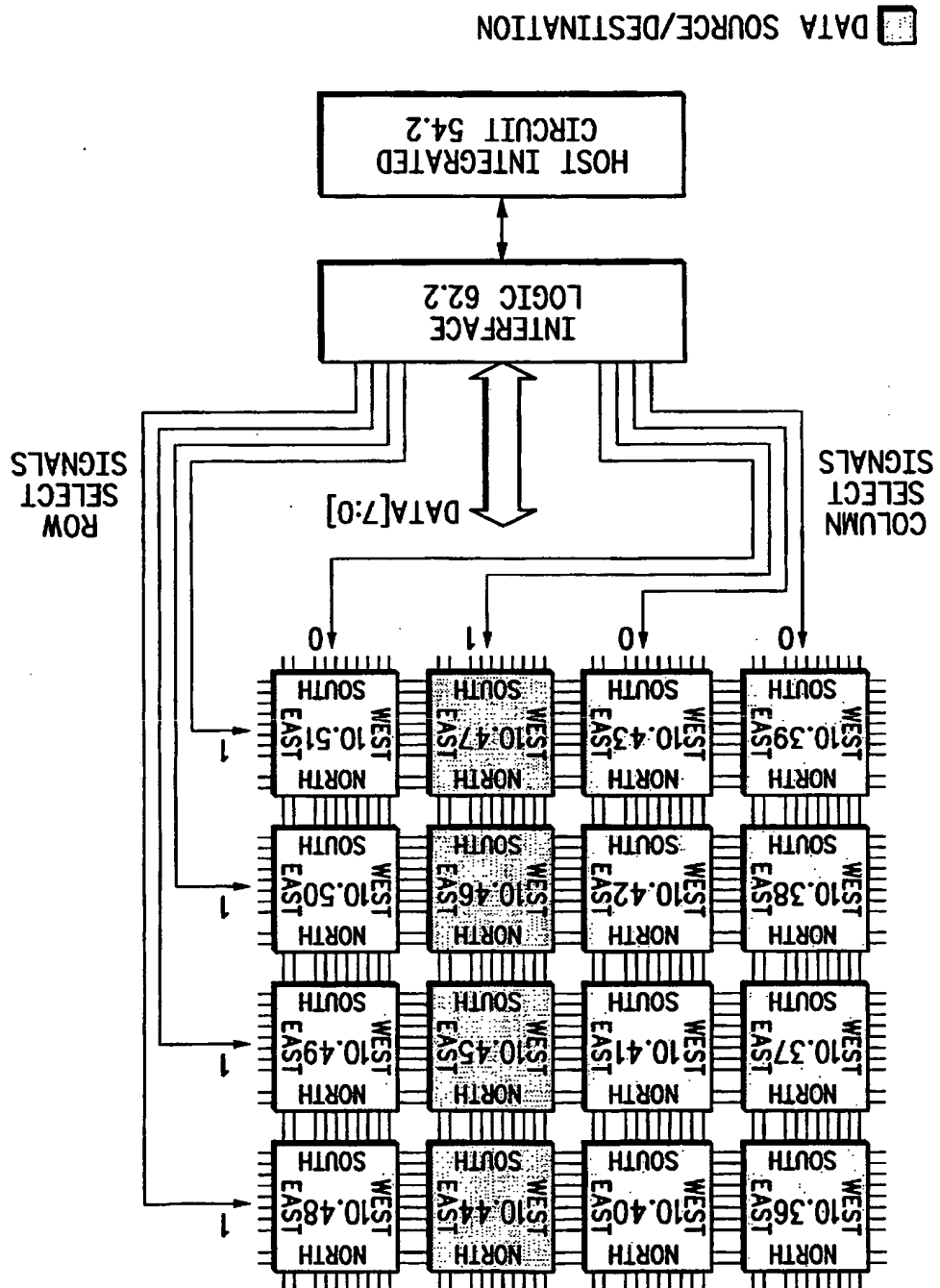
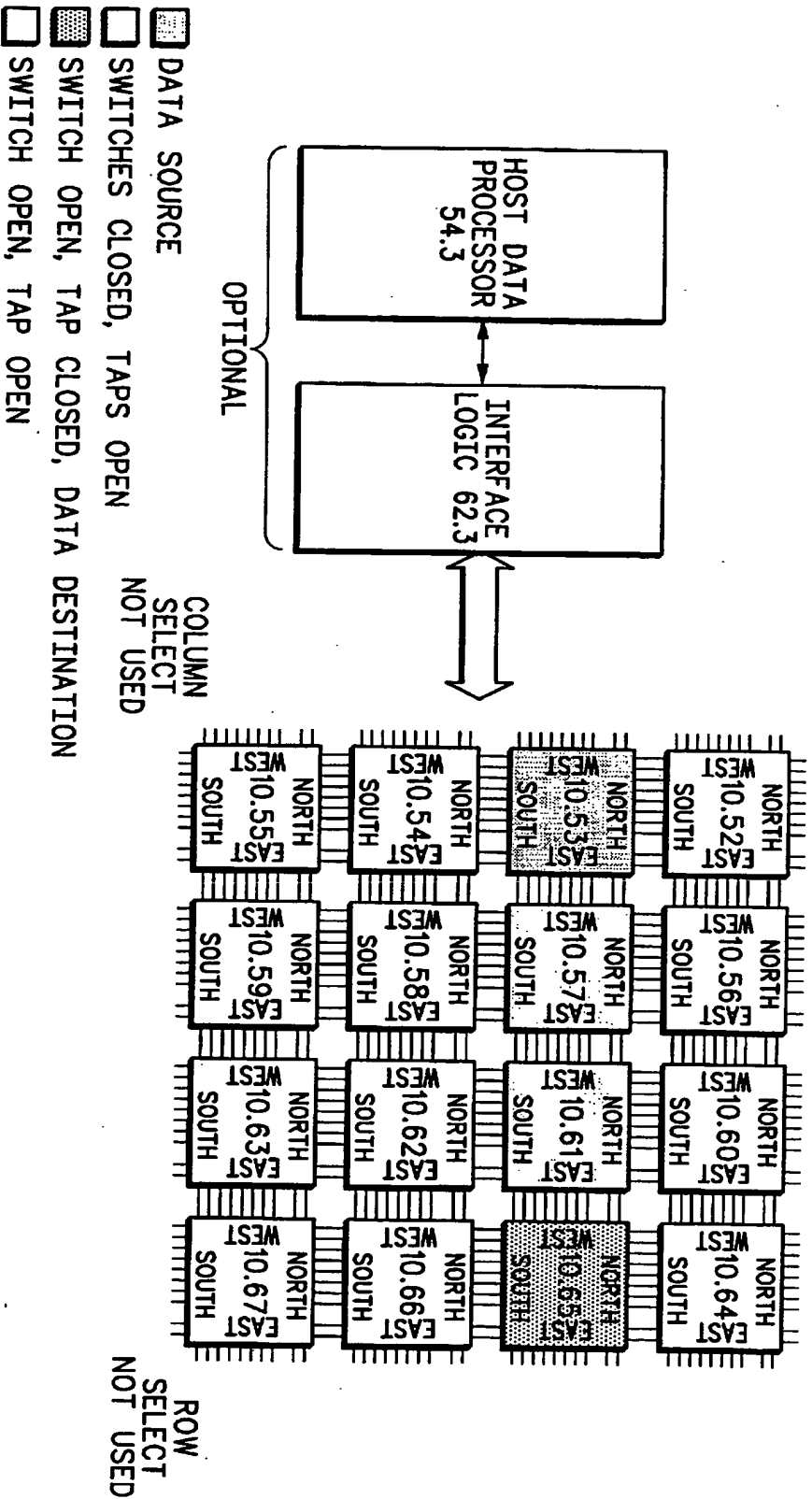


FIG. 56
DATA PROCESSING SYSTEM 55.2

	Docum ent ID	U	Title	Current OR
22	US 60385 84 A	<input checked="" type="checkbox"/>	Synchronized MIMD multi-processing system and method of operation	709/248
23	US 60162 70 A	<input checked="" type="checkbox"/>	Flash memory architecture that utilizes a time-shared address bus scheme and separate memory cell access paths for simultaneous read/write operations	365/185 .11
24	US 59336 24 A	<input checked="" type="checkbox"/>	Synchronized MIMD multi-processing system and method inhibiting instruction fetch at other processors while one processor services an interrupt	709/400
25	US 59059 67 A	<input checked="" type="checkbox"/>	Timing generator with multiple coherent synchronized clocks	702/118
26	US 58812 72 A	<input checked="" type="checkbox"/>	Synchronized MIMD multi-processing system and method inhibiting instruction fetch at other processors on write to program counter of one processor	709/400
27	US 58092 88 A	<input checked="" type="checkbox"/>	Synchronized MIMD multi-processing system and method inhibiting instruction fetch on memory access stall	709/400
28	US 57686 09 A	<input checked="" type="checkbox"/>	Reduced area of crossbar and method of operation	712/11
29	US 57581 95 A	<input checked="" type="checkbox"/>	Register to memory data transfers with field extraction and zero/sign extension based upon size and mode data corresponding to employed address register	712/300
30	US 56969 13 A	<input checked="" type="checkbox"/>	Unique processor identifier in a multi-processing system having plural memories with a unified address space corresponding to each processor	710/317
31	US 56131 46 A	<input checked="" type="checkbox"/>	Reconfigurable SIMD/MIMD processor using switch matrix to allow access to a parameter memory by any of the plurality of processors	712/20
32	US 56065 20 A	<input checked="" type="checkbox"/>	Address generator with controllable modulo power of two addressing capability	708/491
33	US 55924 05 A	<input checked="" type="checkbox"/>	Multiple operations employing divided arithmetic logic unit and multiple flags register	708/518
34	US 55600 29 A	<input checked="" type="checkbox"/>	Data processing system with synchronization coprocessor for multiple threads	712/25
35	US 55220 83 A	<input checked="" type="checkbox"/>	Reconfigurable multi-processor operating in SIMD mode with one processor fetching instructions for use by remaining processors	712/22
36	US 55106 89 A	<input checked="" type="checkbox"/>	Air gap flux measurement using stator third harmonic voltage	318/809
37	US 54715 92 A	<input checked="" type="checkbox"/>	Multi-processor with crossbar link of processors and memories and method of operation	709/213
38	US 54308 50 A	<input checked="" type="checkbox"/>	Data processing system with synchronization coprocessor for multiple threads	709/314
39	US 54106 49 A	<input checked="" type="checkbox"/>	Imaging computer system and network	345/505
40	US 53718 96 A	<input checked="" type="checkbox"/>	Multi-processor having control over synchronization of processors in mind mode and method of operation	712/20
41	US 53394 47 A	<input checked="" type="checkbox"/>	Ones counting circuit, utilizing a matrix of interconnected half-adders, for counting the number of ones in a binary string of image data	377/82
42	US 52724 29 A	<input checked="" type="checkbox"/>	Air gap flux measurement using stator third harmonic voltage and uses	318/808
43	US 52396 54 A	<input checked="" type="checkbox"/>	Dual mode SIMD/MIMD processor providing reuse of MIMD instruction memories as data memories when operating in SIMD mode	712/20
44	US 52261 25 A	<input checked="" type="checkbox"/>	Switch matrix having integrated crosspoint logic and method of operation	710/317

RUN MODE DATA OPERATIONS



DATA PROCESSING SYSTEM 55.3

FIG. 5-7

	Docum ent ID	U	Title	Current OR
45	US 52127 77 A	<input checked="" type="checkbox"/>	Multi-processor reconfigurable in single instruction multiple data (SIMD) and multiple instruction multiple data (MIMD) modes and method of operation	712/229
46	US 51971 40 A	<input checked="" type="checkbox"/>	Sliced addressing multi-processor and method of operation	711/220

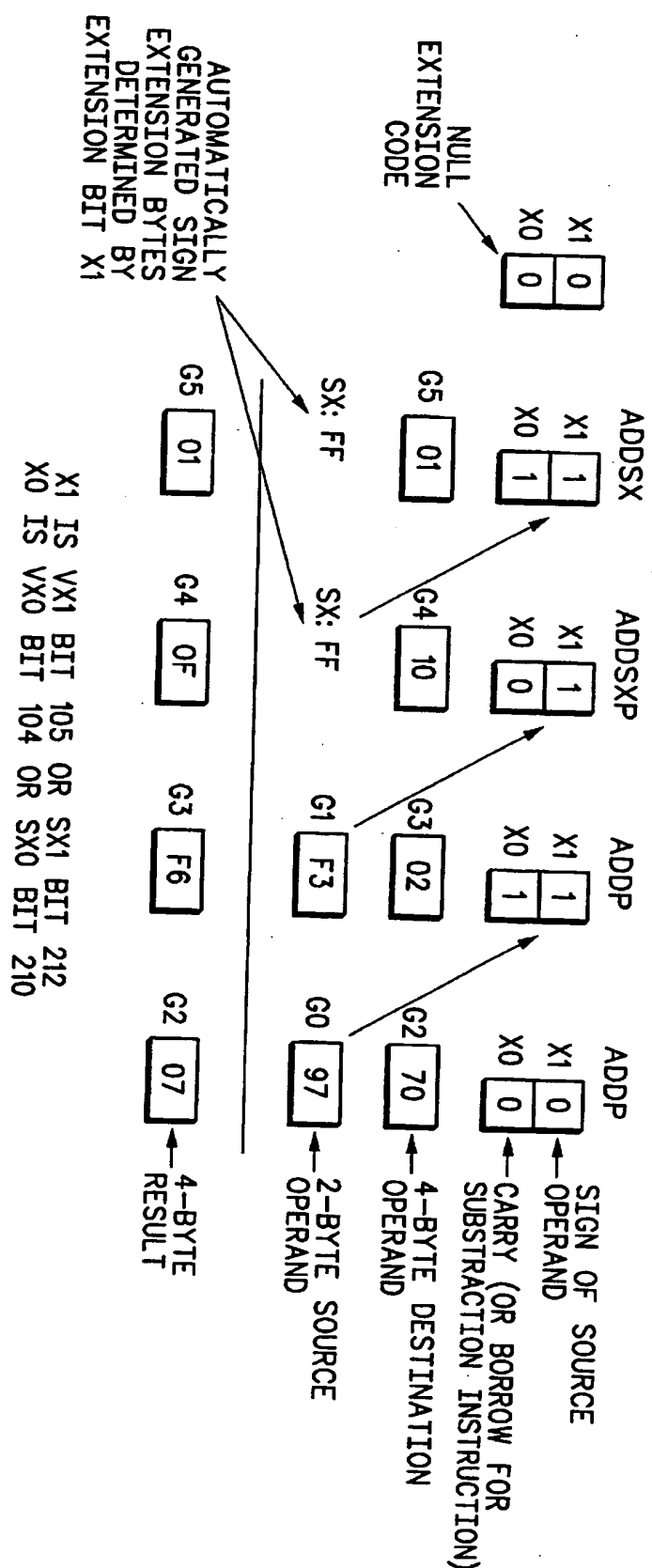


FIG. 5-8